AN10847

Doherty RF performance analysis using the BLF6G20-230PRN

Rev. 01 — 29 January 2010 Application note

Document information

Info	Content
Keywords	RF power transistors, Doherty amplifiers, main amplifier, peak amplifier, AB amplifiers, RF performance, Digital PreDistortion (DPD), base station applications, BLF6G20-230PRN, 1800 MHz to 1880 MHz, W-CDMA, GMSK, EDGE
Abstract	The high power and high-efficiency architecture of the Doherty amplifier coupled with ease of implementation provides service providers with increased efficiency at reduced operating costs for high peak-to-average ratio (PAR) signals. This has made Doherty amplifiers the preferred option in W-CDMA base stations and multi-carrier applications. This application note describes the RF performance analysis of a Doherty amplifier, using a BLF6G20-230PRN transistor.

Revision history

Rev	Date	Description
01	20100129	Initial version

Contact information

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1. Introduction

Developed by W.H. Doherty in 1936, the Doherty amplifier remained largely dormant because the dominant mobile communication system modulation techniques (FM, GMSK and EDGE) did not require high peak-to-average ratio (PAR) signals. Today, however, the high power added efficiency architecture of the Doherty amplifier coupled with ease of implementation provides service providers with increased efficiency at reduced operating costs for high peak-to-average ratio (PAR) signals. This has made Doherty amplifiers the preferred option in W-CDMA base stations and multi-carrier applications for today's service providers.

The BLF6G20-230PRN transistor is a 230 W LDMOS power transistor designed specifically for use in base station applications at frequencies between 1800 MHz and 2000 MHz. In the Doherty configuration described in this application note, the BLF6G20-230PRN operates with section one operating as the main amplifier and section two operating as the peak amplifier. Both sections are internally matched for ease of use and protected against ESD by integrated protection diodes.

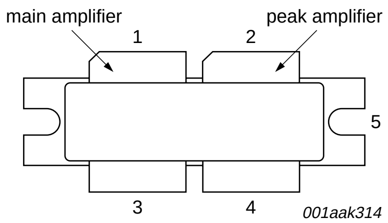
Doherty amplifiers are becoming dominant in W-CDMA base stations and multi-carrier applications because of their enhanced efficiency but there is a trade-off; the linearity and gain are lower than standard class AB amplifiers. However, advancements in Digital PreDistortion (DPD) reduce Doherty amplifier distortion. When combined with optimal device and amplifier design, the decrease in linearity is significantly reduced.

This application note describes the typical RF performance obtainable with a BLF6G20-230PRN Power LDMOS transistor in a DCS (1805 MHz to 1880 MHz) Doherty amplifier configuration.

2. Transistor and analysis details

The transistor and parameter set for the analyses were:

- Transistor: BLF6G20-230PRN
- Frequency band: 1805 MHz to 1880 MHz
- Modulation: 4-carrier EDGE and GMSK
- PCB number: 1030



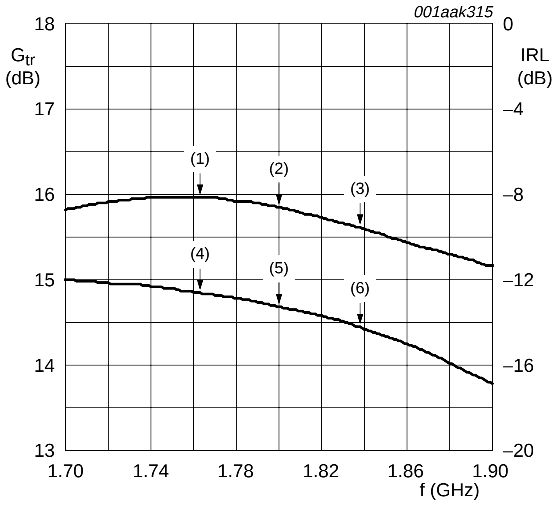
Drain1 = 1, drain2 = 2, gate1 = 3, gate2 = 4 and source = 5

Fig 1. Footprint of the BLF6G20-230PRN showing the two Doherty amplifier sections

The performance analyses were performed as follows:

- Gain, IRL and group delay measured using P_L = 47.5 dBm, V_{DS} = 32 V, I_{Dq} = 1400 mA (main amplifier) and V_{GS} = 0.7 V (peak amplifier)
- 4-carrier GMSK measured using V_{DS} = 32 V, I_{Dq} = 1400 mA (main amplifier) and V_{GS} = 0.7 V (peak amplifier)
- 4-carrier EDGE were measured using V_{DS} = 32 V, I_{Dq} = 1400 mA (main amplifier) and V_{GS} = 0.7 V (peak amplifier)
- Peak power was recorded using a pulsed Continuous Wave (CW) signal under the following operating conditions: 12 μs pulse width at 10 % duty cycle, V_{DS} = 32 V, I_{Dq} = 1400 mA (main amplifier) and V_{GS} = 0.7 V (peak amplifier)

2.1 RF performance analysis



Bias: V_{DS} = 32 V, I_{Dq} = 1400 mA (main amplifier), V_{GS} = 0.7 V (peak amplifier), start frequency = 1.742500 GHz, stop frequency = 1.942500 GHz.

(1) G_{tr} = 1.805 GHz at 15.970 dB.

(2) G_{tr} = 1.842 GHz at 15.846 dB.

(3) G_{tr} = 1.880 GHz at 15.609 dB.

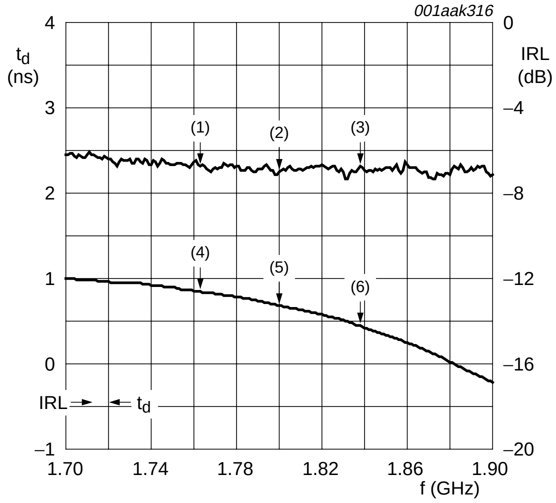
(4) IRL = 1.805 GHz at –12.6186 dB.

(5) IRL = 1.842 GHz at –13.266 dB.

(6) IRL = 1.880 GHz at –14.230 dB.

Fig 2. Transducer power gain (G_{tr}) in dB and IRL in dB over the frequency range

Figure 2 shows a gain flatness of < 0.4 dB between 1805 MHz and 1880 MHz.



Bias: V_{DS} = 32 V, I_{Dq} = 1400 mA (main amplifier), V_{GS} = 0.7 V (peak amplifier), start frequency = 1.742500 GHz, stop frequency = 1.942500 GHz, td = electrical delay.

(1) t_d = 1.845 GHz at 2.313 ns.

(2) t_d = 1.842 GHz at 2.250 ns.

(3) t_d = 1.880 GHz at 2.316 ns.

(4) IRL = 1.805 GHz at –12.619 dB.

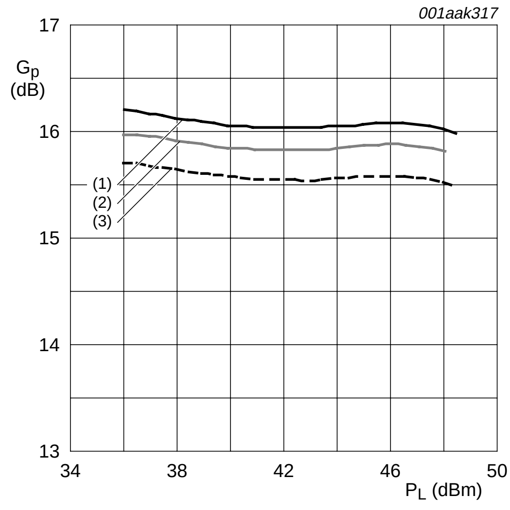
(5) IRL = 1.842 GHz at –13.266 dB.

(6) IRL = 1.880 GHz at –14.230 dB.

Fig 3. Electrical delay in ns and IRL in dB against the frequency range

2.2 4-carrier GMSK analysis

- Test Signal: 4-carrier GSM, 3 MHz spacing and PAR = 6.1 dB at 0.01 % probability on the CCDF
- IMD3: measured at 7.5 MHz offset from the central frequency
- IMD5: measured at 10.5 MHz offset from the central frequency



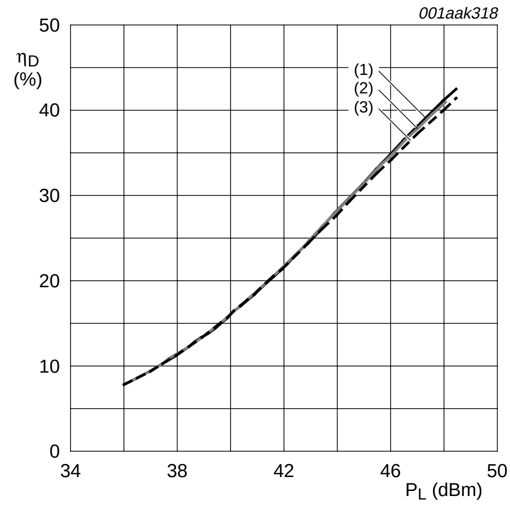
Bias: V_{DS} = 32 V, I_{Dq} = 1400 mA (main amplifier), V_{GS} = 0.7 V (peak amplifier).

(1) 1805 MHz.

(2) 1842.5 MHz.

(3) 1880 MHz.

Fig 4. Power gain as a function of output power; 4-carrier GMSK



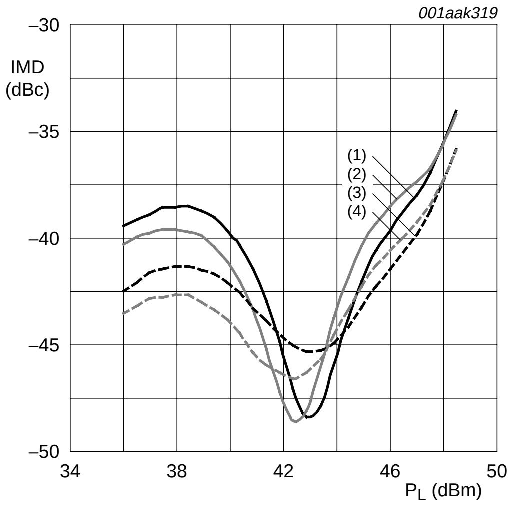
Bias: V_{DS} = 32 V, I_{Dq} = 1400 mA (main amplifier), V_{GS} = 0.7 V (peak amplifier).

(1) 1805 MHz.

(2) 1842.5 MHz.

(3) 1880 MHz.

Fig 5. Drain efficiency as a function of output power; 4-carrier GMSK



Bias: V_{DS} = 32 V, I_{Dq} = 1400 mA (main amplifier), V_{GS} = 0.7 V (peak amplifier).

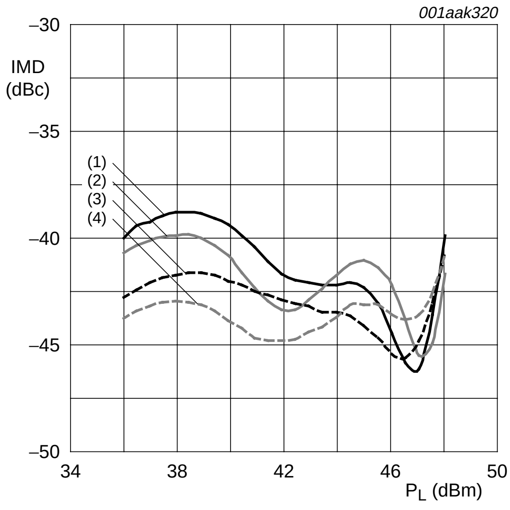
(1) IMD3 low.

(2) IMD3 high.

(3) IMD5 low.

(4) IMD5 high.

Fig 6. IMD3 and IMD5 as a function of output power; 4-carrier GMSK at 1805 MHz



Bias: V_{DS} = 32 V, I_{Dq} = 1400 mA (main amplifier), V_{GS} = 0.7 V (peak amplifier).

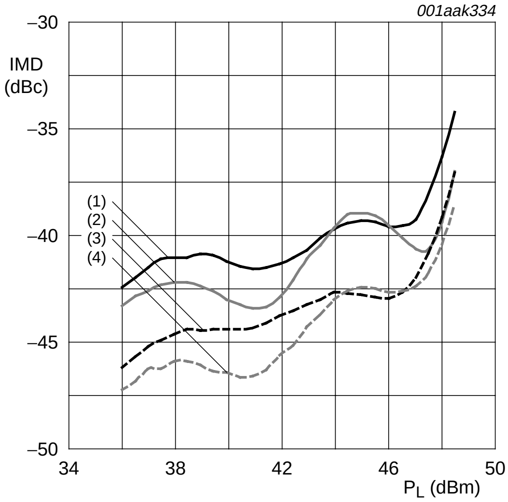
(1) IMD3 low.

(2) IMD3 high.

(3) IMD5 low.

(4) IMD5 high.

Fig 7. IMD3 and IMD5 as a function of output power; 4-carrier GMSK at 1842.5 MHz



Bias: V_{DS} = 32 V, I_{Dq} = 1400 mA (main amplifier), V_{GS} = 0.7 V (peak amplifier).

(1) IMD3 low.

(2) IMD3 high.

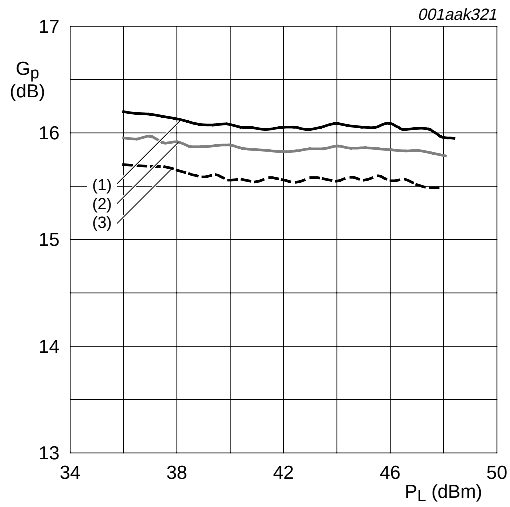
(3) IMD5 low.

(4) IMD5 high.

Fig 8. IMD3 and IMD5 as a function of output power; 4-carrier GMSK at 1880 MHz

2.3 4-carrier EDGE analysis

- Test Signal: 4-carrier GSM, 3 MHz spacing and PAR = 8.2 dB at 0.01 % probability on the CCDF
- IMD3: measured at 7.5 MHz offset from the central frequency
- IMD5: measured at 10.5 MHz offset from the central frequency



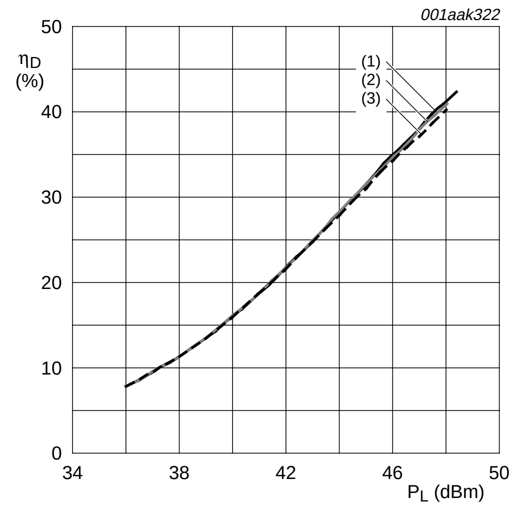
Bias: V_{DS} = 32 V, I_{Dq} = 1400 mA (main amplifier), V_{GS} = 0.7 V (peak amplifier).

(1) 1805 MHz.

(2) 1842.5 MHz.

(3) 1880 MHz.

Fig 9. Gain as a function of output power; 4-carrier EDGE



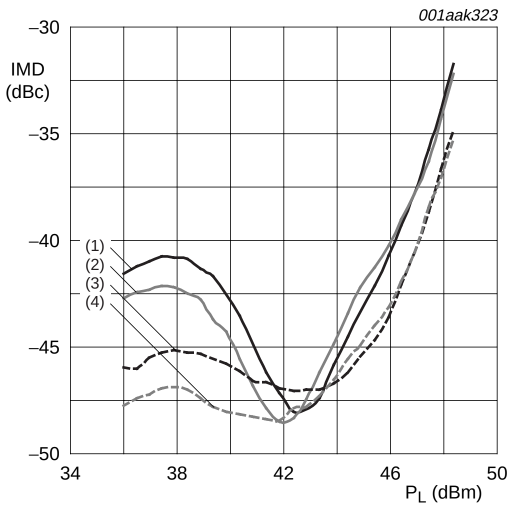
Bias: V_{DS} = 32 V, I_{Dq} = 1400 mA (main amplifier), V_{GS} = 0.7 V (peak amplifier).

(1) 1805 MHz.

(2) 1842.5 MHz.

(3) 1880 MHz.

Fig 10. Drain efficiency as a function of output power; 4-carrier EDGE



Bias: V_{DS} = 32 V, I_{Dq} = 1400 mA (main amplifier), V_{GS} = 0.7 V (peak amplifier).

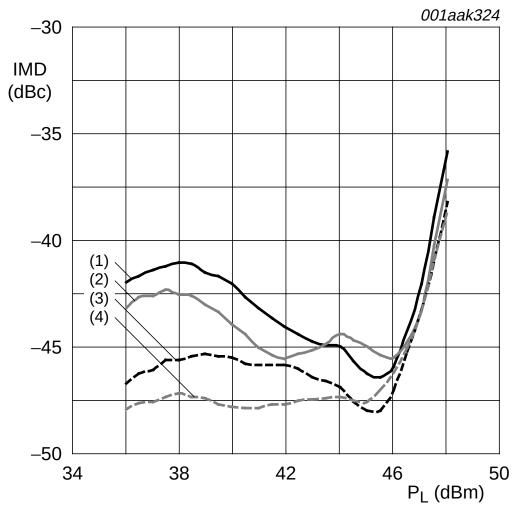
(1) IMD3 low.

(2) IMD3 high.

(3) IMD5 low.

(4) IMD5 high.

Fig 11. IMD3 and IMD5 as a function of output power; 4-carrier EDGE at 1805 MHz



Bias: V_{DS} = 32 V, I_{Dq} = 1400 mA (main amplifier), V_{GS} = 0.7 V (peak amplifier).

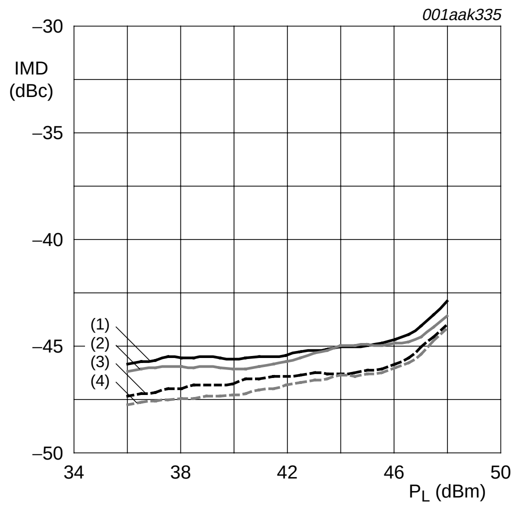
(1) IMD3 low.

(2) IMD3 high.

(3) IMD5 low.

(4) IMD5 high.

Fig 12. IMD3 and IMD5 as a function of output power; 4-carrier EDGE at 1842.5 MHz



Bias: V_{DS} = 32 V, I_{Dq} = 1400 mA (main amplifier), V_{GS} = 0.7 V (peak amplifier).

(1) IMD3 low.

(2) IMD3 high.

(3) IMD5 low.

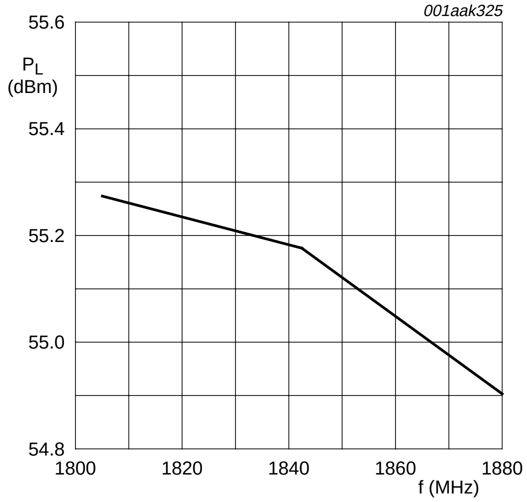
(4) IMD5 high.

Fig 13. IMD3 and IMD5 as a function of output power; 4-carrier EDGE at 1880 MHz

2.4 Peak power capability analysis

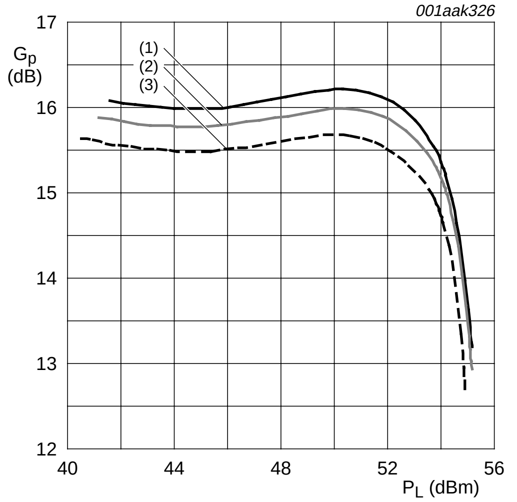
There are two methods for analyzing peak power:

- Using a standard IS95 signal (PAR = 9.7 dB at 0.01 % probability on the CCDF). Determine the output power (P_L) when the Peak-to-Average power Ratio (PAR) reaches a value of 6.7 dB at 0.01 % probability on the CCDF. This is called the 3 dB compression point. See Figure 14 for more information.
- Using the pulsed signal and measuring the 3 dB compression points. See Figure 15 for more information.
- 12 µs Pulse width and 10 % duty cycle



Bias: V_{DS} = 32 V, I_{Dq} = 1400 mA (main amplifier), V_{GS} = 0.7 V (peak amplifier).

Fig 14. Output power of the IS95 signal as a function of frequency



Bias: V_{DS} = 32 V, I_{Dq} = 1400 mA (main amplifier), V_{GS} = 0.7 V (peak amplifier).

(1) 1805 MHz.

(2) 1842.5 MHz.

(3) 1880 MHz.

Fig 15. Pulse signal power gain as a function of output power

3. Bill of materials for a Doherty configuration using a BLF6G20-230PRN

Table 1. Bill of materials for a Doherty configuration using a BLF6G20-230PRN

PCB material: Rogers 3006 (see Ref. 1 on page 15); ε_r = 6.15 ± 0.15; thickness 0.64 mm (0.025"); 35 μm (1 oz.) copper on each side.

Designator	Description	Part number	Manufacturer
Q1, Q2	7808 Voltage Regulator	NJM#78L08UA-ND	NJR
Q3, Q4	2N2222 NPN Transistor	-	NXP Semiconductors
L1, L2, L3, L4	Ferroxcube Bead	2743019447	Fair Rite
L5, L6	5.6 nH Inductor	0805HQ-5N6X	Coilcraft
L7, L8	3.6 nH Inductor	0603CS-3N6X	Coilcraft
C1, C2, C6, C7, C34, C35	1 μF Ceramic Chip Capacitor	GRM31MR71H105K88L	MuRata
C3, C4, C5, C8, C9, C10	100 nF Ceramic Chip Capacitor	S0805W104K1HRN-P4	Multicomp
C15, C18, C27, C28	1 μF Ceramic Chip Capacitor	GRM31CR72A105KA0	MuRata
C17, C21, C22, C30	10 μF Ceramic Chip Capacitor	GRM32ER7YA106K88L	MuRata
C11, C12, C13, C14	15 pF ATC100B	ATC100B150JT500X	American Technical Ceramics
C16, C20, C25, C29	15 pF ATC100B	ATC100B150JT500X	American Technical Ceramics
C19, C26	0.4 pF ATC100B	ATC100B0R4JT500X	American Technical Ceramics
C23, C24	0.1 pF ATC100A	ATC100A0R1JT500X	American Technical Ceramics
C31	0.5 pF ATC100B	ATC100B0R5JT500X	American Technical Ceramics
C32, C33	220 μF, 50 V SMT Electrolytic Capacitor	PCE3474CT-ND	Panasonic
D1, D2	0805 Green SMT LED	APT2012CGCK	KingBright
H1	90° Hybrid Coupler	1P503S	Anaren
R1, R30	200 Ω Potentiometer	3214W-1-201E	
R2, R19	2 kΩ Resistor	CRCW08052K00FKTA	Vishay Dale
R3	75 Ω Resistor	CRCW080575R0FKTA	Bourns
R4, R5, R21, R22	432 Ω Resistor	CRCW0805432RFKEA	Vishay Dale
R7, R13, R14, R15, R16, R27	9.1 Ω Resistor	CRCW08059R09FKEA	Vishay Dale
R8, R26	5.1 Ω Resistor	CRCW08055R11FKEA	Vishay Dale
R9, R25	11 kΩ Resistor	CRCW080511K0FKEA	Vishay Dale
R10, R24	1.1 kΩ Resistor	CRCW08051K10FKEA	Vishay Dale
R11, R29	910 Ω Resistor	CRCW0805909RFKTA	Vishay Dale
R12, R28	5.1 kΩ Resistor	CRCW08055K10FKTA	Vishay Dale
R20	0 Ω Resistor	-	Vishay Dale
R31	50 Ω Terminator	2010TALNF	EMC Technology

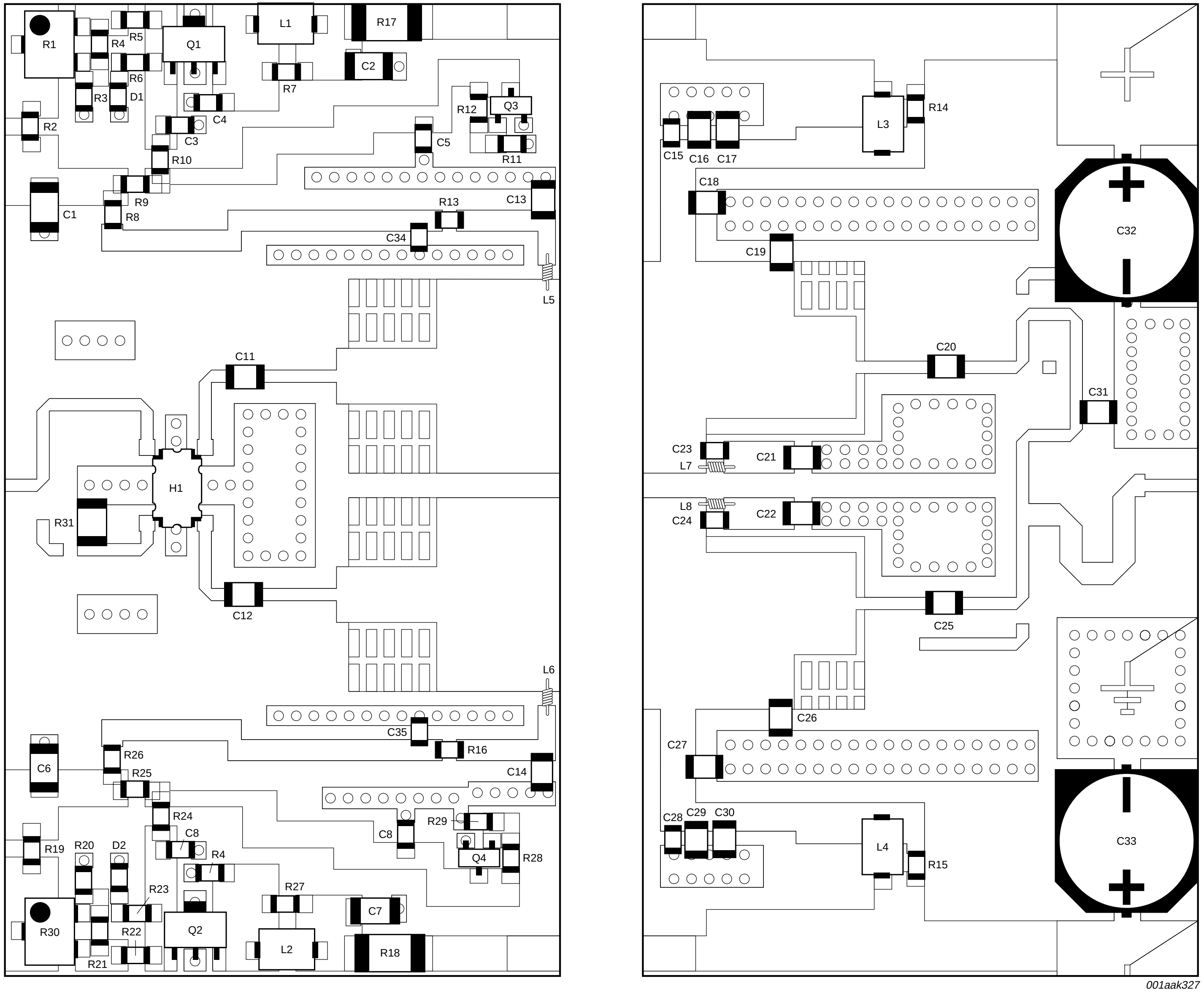


Fig 16. Test board 1030 PCB Layout

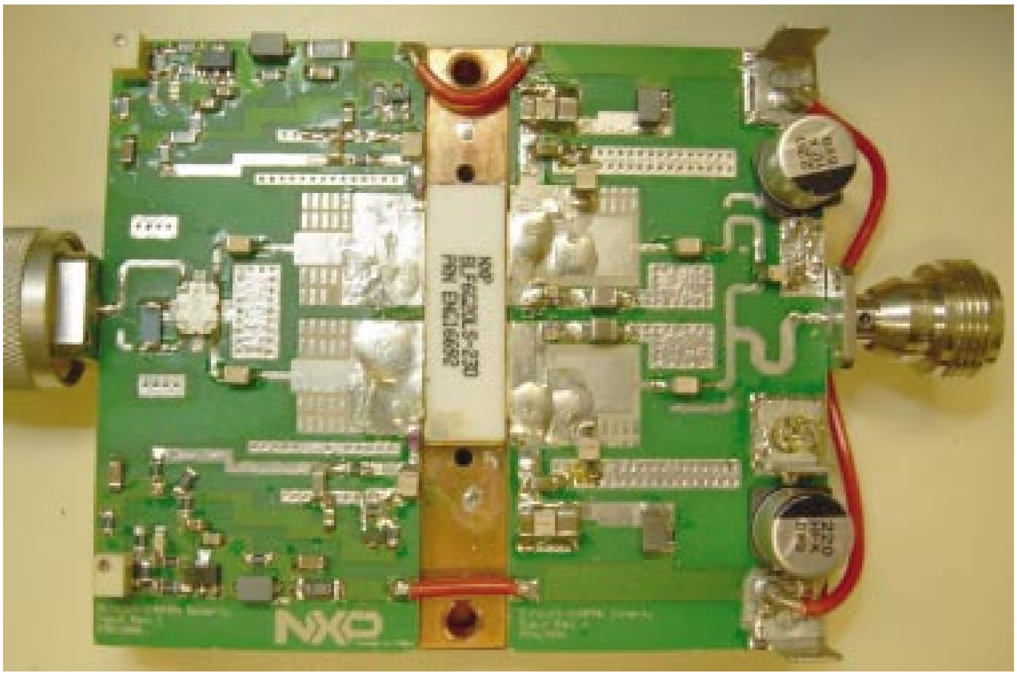


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Fig 17. Test board 1030 with BLF6G20-230PRN

4. Summary and conclusions

4.1 Summary

This application note described a turn-key power amplifier solution, based on the BLF6G20-230PRN high-efficiency LDMOS transistor for multicarrier systems in the range 1805 MHz to 1880 MHz.

Using the symmetrical Doherty architecture enables the design of a highly efficient amplifier for signals with relatively high Peak-To-Average ratios. The amplifier exhibits good peak power of 55 dBm at V_{DS} = 32 V and pre-distortion characteristics.

4.2 Conclusion

The BLF6G20-230PRN operated as a compact two section device:

- Section one operated as the main amplifier
- Section two operated as the peak amplifier

The result was that the amplifier achieves good power and gain characteristics (55 dBm peak power at V_{DS} = 32 V).

5. Abbreviations

Table 2. Abbreviations table

Acronym	Description
CCDF	Complementary Cumulative Distribution Function
DCS	Digital Cellular System
EDGE	Enhanced Data GSM Environment
ESD	ElectroStatic Discharge
GMSK	Gaussian Minimum Shift Keying
IRL	Input Return Loss
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
PAR	Peak-to-Average power Ratio

6. References

[1] **Data sheet 1.3000; RO3000 Series High Frequency Circuit Materials** – Advanced Circuit Materials Division; Rogers Corporation.

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8. Figures

9. Contents

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Date of release: 29 January 2010
Document identifier: AN10847_1